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OBJECTIVE: To work in an academic environment, that will provide me a good platform to utilize my teaching skill and will help me to enhance my research activities for scientific applications by providing me enough space for independent and innovative thinking.

ACADEMIC QUALIFICATION:

Ø **Ph.D. (Awarded on 5th December, 2018):**

Registration No: 0901121000515 (13-08-2015)

University: Institute of Radio Physics and Electronics, University of Calcutta.

Supervisors: i) **Dr. Soma Barman**, Associate Professor, Institute of Radio Physics and Electronics, University of Calcutta and ii) **Dr. Jaydeb Bhaumik**, Professor, Electronics and Telecommunication Engineering, Jadavpur University.

Duration: 13/03/2015 – 05/12/2018 (Submission: 10th Nov, 2017, Defence: 29th November, 2018)

Thesis Title: Design and Implementation of Error Correcting Codes

Thesis Summary: This thesis presents some new design techniques and efficient VLSI implementation of binary and non-binary ECCs like single error correction (SEC) codes, single error correction-double error detection (SEC-DED) codes, Reed-Solomon (RS) codes, cellular automata (CA) based ECC for digital communication and memory systems like CD, ultra-wide band, Intelligent home networking systems. Different bit and byte error correcting codes have been developed to increase the reliability of memory systems and stored DNA sequences.

- Ø **M.TECH (Gold Medalist): (ECE)**
University: West Bengal University of Technology
Grade: 9.63/10 (DGPA) (88.80%), 26/07/2008
Duration: 2006-2008
Thesis Title: Delay and power estimation model for UDSM VLSI circuits.
Thesis Summary: Estimate the delay and power models of CMOS VLSI circuits, when the channel length in the order of ultra submicron range. Also verify our estimated result with latest simulation tool like Cadence.
- Ø **B.TECH: (ECE)**
University: West Bengal University of Technology
Grade: 8.65/10 (DGPA) (79.00%), 08/07/2005
Duration: 2001-2005
Project Title: “Processed Power Distribution”
Project Summary: To control the amplitude and the frequency of power supply at the substation.
- Ø **Higher Secondary** (H.S.-10+2) from Jalchak N. N. Vidyayatan under West Bengal Council of Higher Secondary Education (W.B.C.H.S.E) with an aggregate of 81.3% in 2000. (June, 2000) **WBJEE Rank (2001):** 3568.
- Ø **Secondary (M.P.-10)** from Shyamsundar Pur R K Vidyapith under West Bengal Board of Secondary Education (W.B.B.S.E) with an aggregate of 83% in 1998. (May, 1998).

PROFESSIONAL EXPERIENCES:

Name of organization	Designation	Duration	Experience (year, months)	Pay Scale, Basic pay
Haldia Institute of Technology, Haldia	Visiting Lecturer	16.01. 2006 to 15.07.2007	1 year 6 months	
Mallbhum Institute of Technology, Bishnupur	Lecturer	16.07. 2007 to 07.07.2008	1 year	8000-275-13500, 8000/-
Haldia Institute of Technology, Haldia	Lecturer	08.07.2008 to 08.09.2010	2 years 2 month	8000-275-13500, 8275/-
Haldia Institute of Technology, Haldia	Assistant Professor (GP-6000/- T1)	09.09.2010 to 08.09.2013	3 years	15600-39100, 23440/
Haldia Institute of Technology, Haldia	Assistant Professor (GP-7000/- T2)	09.09.2013 to 08.09.2018	5 years	15600-39100, 28370/
Haldia Institute of Technology, Haldia	Assistant Professor (GP-8000/- T3)	09.09.2018 to 31.03.2019	7 months	15600-39100, 32920/-
Haldia Institute of Technology, Haldia	Associate Professor (GP-9000/- T4)	01.04.2019 to till date	6 years 2 months	37400-67000, 53820/-

RESEARCH AND PUBLICATIONS:

Research Interests: Digital VLSI Design, VLSI architecture for Error Correcting Codes, Fault Tolerant Storage or Memory Systems, Cellular Automata, Cryptography

Patents:

1. S. Balamurugan, G. V. Gopal, Dr. Shailendra Kumar Pareek, **Jagannath Samanta**, Tarun Kumar Ghosh, Pankaj Jain, Shrikrishna Dhakad, Gedela Jagga Rao, Rajesh Purohit: Machine Learning Based Emotion Recognition and Recommendation System by Analysing ECG Signals. Application number: 202341005843, Date of File: 30-01-2023, Journal Number: 07/2023, Publication date: 17/02/2023, pp.11400, Office of the Controller General of Patents, Designs and Trade Marks, Govt. of India

2. S. Barman, S. Koley, P.P. Acharjya, **J. Samanta**, M. Sen, S. Jana, R.K. maity, S. Bijali Maity, A. Paria: A Method for Efficient Optimization of Clustering in Adhoc Networks through Genetic Algorithm, Application number: 202331067251 A, Date of File: 06-10-2023, Journal Number: 42/2023, Publication date: 20/10/2023 pp.72835, Office of the Controller General of Patents, Designs and Trade Marks, Govt. of India

3. S. Jaywant, Y. M. S. Negi, P. Sharma, S. Bardhan, **J. Samanta**, T. Sinha Roy, J. Yadavrao Hire, S. Das, S. Dasgupta, A. R Jamader: Digital Chopping Board For Kitchen, Design Application number: 438173-001, Cbr Number:221514, Cbr Date: 22-11-2024, Journal No is 07/2025, Publication date: 14/02/2025, Office of the Controller General of Patents, Designs and Trade Marks, Govt. of India, Granted (12-02-2025)

A. Journal Publication: (SCIE=13, Scopus=6, ESCI=4, Others=8) International Journal

- [1] B P De and **J. Samanta**, “*Thermal bound placement with wire length consideration for standard cells in VLSI*”, IJCSI International Journal of Computer Science Issues, Special Issue, ICVCI-2011, vol. 1, no. 1, pp:19-22, ISSN: 1694-0814, November 2011. I.F.=0.242, <http://www.ijcsi.org/papers/IJCSI-ICVCI-2011-19-22.pdf>
- [2] **J. Samanta**, B. P. De, B. Bag & R. K. Maity, “*Comparative study for delay & power dissipation of CMOS Inverter in UDSM range*”, International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, vol.-1, no.-6, pp:162-167, January 2012. I.F.=1.0
http://www.ijscce.org/attachments/File/Vol-1_Issue-6/F0290111611.pdf
- [3] R. K. Maity, **J. Samanta**, “*Construction and performance studies of a pseudo-orthogonal code for fiber optic CDMA LAN*”, International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, vol.-1, no.-6, pp: 196-201, January 2012. I.F.=1.0
http://www.ijscce.org/attachments/File/Vol-1_Issue-6/F0297111611.pdf
- [4] **J. Samanta**, A Patra, D Mishra, R Rashmi, I Kundu & R Koley, “*Performance Analysis of Different Topologies of 1-Bit Full Adder in UDSM Technology*”, International Journal of Innovative Technology and Exploring Engineering

- (IJITEE) ISSN: 2278-3075, vol.-1, no.-2, pp:35-42, July-2012. I.F.=1.0, <http://www.ijitee.org/attachments/File/v1i2/B0143061212.pdf>.
- [5] **Jagannath Samanta**, Mousam Halder, Bishnu Prasad De, “*Performance Analysis of High Speed Low Power Carry Look-Ahead Adder Using Different Logic Styles*” International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, vol.-2, no.-6, pp:330-336, Jan- 2013. I.F.=1.0
http://www.ijscce.org/attachments/File/v2i6/IJSCE_NCACD_2.pdf
- [6] Jaydeb Bhaumik, Anindya Sundar Das and **Jagannath Samanta**, “*Architecture for Programmable Generator Polynomial Based Reed-Solomon Encoder and Decoder*” International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, vol.-2, no.-6, pp:395-399, Jan- 2013. I.F.=1.0
http://www.ijscce.org/attachments/File/v2i6/IJSCE_NCACD_17.pdf
- [7] Razia Sultana and **Jagannath Samanta**, “*Comparison of different design techniques of XOR & AND gate using EDA simulation tool*”, International Journal of VLSI and Embedded Systems (IJVES), ISSN: 2249-6556, vol.-4, no.-3, pp:343-349, May - June 2013. I.F.=1.29, http://ijves.com/?page_id=469
- [8] M. Basak, M. Sutradhar, B. Santra, M. Saha, D. Chowdhury and **J. Samanta**, “*Study the performance analysis of low power –high speed carry select adder using EDA simulation tool*”, International Journal of VLSI and Embedded Systems (IJVES), ISSN: 2249-6556, vol.-4, Article-06102, pp:444-448, June 2013., I.F.=1.29
http://ijves.com/?page_id=546.
- [9] **Jagannath Samanta** and Jaydeb Bhaumik, “*Comments On VLSI Implementation Of Reed-Solomon Encoder Algorithm For Communication Systems*” in Radioelectronics and Communications Systems, (**Springer**), ISSN: 1934-8061, vol. 57, no. 7, pp:331-332, July, 2014. (**SCImago, IF-0.19, Q3**). DOI:10.3103/S0735272714070061
- [10] Madhuresh Suman, **Jagannath Samanta**, Dibyendu Chowdhury and Jaydeb Bhaumik., “*Relative Performance Analysis of Different CMOS Full Adder Circuits*”, International Journal of Computer Applications, ISSN: 0975 – 8887, vol. 114, no. 6, pp:8-14, March 2015., I.F.=0.752, 973-93-80885-73-1.
<http://www.ijcaonline.org/archives/volume114/number6/19981-1922>
- [11] **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, CA-based Area Optimized Three Bytes Error Detecting Codes, in Journal of Cellular Automata (Old City Publishing), (**SCI Expanded, IF-0.698, Q3**), vol.10, no.5-6, pp:409-423, Oct.-2015. ISSN: 1557-5969.
- [12] **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, Modified Karatsuba multiplier for ‘key equation solver’ in RS code, in Radioelectronics and Communications Systems Journal (Springer), vol. 58, no.10, pp:452-461, 2015. (**SCImago, IF-0.19, Q3**). DOI: 10.3103/S0735272715100039.
- [13] **J. Samanta**, J. Bhaumik and Soma Barman, A transistor level implementation of Reed Solomon encoder in $GF(2^8)$, in Journal of active and passive electronics devices (Old City Publishing), (**ESCI, Web of Science, UGC Approved**) vol-11, no. 2-3, pp:243-261, 2016. ISSN: 1555-0281.
- [14] **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, “FPGA based Area Efficient RS(23, 17) Codec”, Microsystem Technologies (Springer, **IF: 0.974, SCIE, Q2**), vol. 23, no.3, pp.639-650, 2017. ISSN: 1432-1858, DOI: 10.1007/s00542-016-3058-1.

- [15] **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, "Compact CA-based single byte error correcting codec", **IEEE Transactions on Computers**, vol.67, no.2, pp.291-298, ISSN: 1557-9956, (**SCI, I.F: 2.916, Q1**), DOI 10.1109/TC.2017.2739726, Aug. 2017.
- [16] **Jagannath Samanta** and Sayan Tripathi, "Comments on "A novel approach of error detection and correction for efficient energy in wireless networks"", **Multimedia Tools and Application**, (**Springer, IF=1.541, SCIE, Q2**), vo. 78, no. 6, pp. 7579–7584, ISSN: 1573-7721, (DOI: 10.1007/s11042-018-6481-8), August, 2018.
- [17] **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, "FPGA and ASIC Implementation of RS(47, 41) Codec for Intelligent Home Networking System", **Journal of Active & Passive Electronic Devices (JAPED)**, Old City Publishing (USA), (**ESCI, Web of Science, UGC Approved**), vol. 13, no.4, p. 317-327, Nov. 2018. ISSN: 1555-0281.
- [18] Tarique Hassan, **Jagannath Samanta** and Jaydeb Bhaumik, FPGA and ASIC Implementation of Different Finite Field Multipliers for Fomey Block, in **Journal of active and passive electronics devices (Old City Publishing)**, vol.14, no.2/3, pp:157-171, August-2019. ISSN: 1555-0281, Accession Number WOS: 000476609100005, (ESCI, Web of Science, **UGC Approved**).
- [19] **J. Samanta**, J. Bhaumik and S. Barman, "Compact and Power Efficient SEC-DED Codec for Computer Memory", **Microsystem Technologies**, (Springer, **IF: 1.581, SCIE, Q2**), vol.27, no.2, pp.359-368, Feb. 2019, ISSN: 1432-1858, DOI: 10.1007/s00542-019-04366-7.
- [20] Raj Kumar Maity, **Jagannath Samanta** and Sweta Bijali Maity, Performance Analysis of A Single Error Correcting (SEC) Code with Different Decoding Techniques, **Journal of Critical Reviews**, ISSN- 2394-5125, **Scopus**, IF=0.39, Vol.7, No. 07, July, 2020, pp. 4175-4179, DOI: 10.31838/jcr.07.07.383.
- [21] Raj Kumar Maity, Sayan Tripathi, Jagannath Samanta and Jaydeb Bhaumik, "Lower complexity error location detection block of adjacent error correcting decoder for SRAMs", **IET Computers & Digital Techniques**, (**SCIE, IF=0.857, Q3**), vol. 14, No. 5, pp.210-216, Sept., 2020. DOI: 10.1049/iet-cdt.2019.0268, Print ISSN 1751-8601, Online ISSN 1751-861X.
- [22] Adhikary, Akash, Tapan Maity, Jagannath Samanta, Sudipta Bardhan and Balaram Dey, "Design and Development of A Smart Parachute Control System for Military and Civilian Applications." **Turkish Journal of Computer and Mathematics Education (TURCOMAT)**, (**Scopus**), IF=0.218, Vol. 11, no. 1 (2020): e-ISSN 1309-4653, pp.492-501.
- [23] Sayan Tripathi, Raj Kumar Maity, Jhila Jana, Jagannath Samanta, Jaydeb Bhaumik, FPGA Based Low Area Multi-bit Adjacent Error Correcting Codec for SRAM Application, in **Radioelectronics and Communications Systems Journal (Springer, Scopus, Q3, IF-0.19)**, ISSN-19348061, vol. 63, no. 10, pp. 543-552, Dec, 2020, 10.3103/S0735272720100040.
- [24] Jagannath Samanta and Akash Kewet, "Compact and High Speed Hsiao Based SEC-DED Code for Cache Memory", **Journal of Circuits, Systems, and Computers (World Scientific)**. (**SCIE, IF=1.363, Q3**), ISSN (print): 0218-1266 | ISSN (online): 1793-6454, Vol-31, No-01, pp:2250004 July, 2021, DOI:10.1142/S0218126622500049.

- [25] Raj Kumar Maity, **Jagannath Samanta**, and Jaydeb Bhaumik, "Construction Techniques and Evaluation of High Performance t-bit Burst Error Correcting Codes for Protecting MCUs, Journal of Circuits, Systems, and Computers. (**SCIE**, **IF=1.278**, **Q3**), Vol. 32, No. 09, 2350142, ISSN (print): 0218-1266 | ISSN (online): 1793-6454, Oct-2022. **DOI**: 10.1142/S0218126623501426.
- [26] Raj Kumar Maity, **Jagannath Samanta**, and Jaydeb Bhaumik, Single and Double-adjacent Error Correcting Code (SDECC) with Lower Design Overheads and Mis-correction Rate for SRAMs, Microsystem Technologies (**SCIE**, **IF=2.012**, **Q2**), 29, pp 823–834 May-2023, **DOI**: 10.1007/s00542-023-05464-3
- [27] Raj Kumar Maity, **Jagannath Samanta**, and Jaydeb Bhaumik, "An Improved Single and Double-Adjacent Error Correcting Codec with Lower Decoding Overheads, Journal of Signal Processing Systems (**SCIE**, **IF=1.813**, **Q2**), 95, pp. 721–733, May-2023, 10.1007/s11265-023-01875-7.
- [28] Sweta Bijali Maity, Raj Kumar Maity, **Jagannath Samanta**, and Chanchal Kumar De, Comments on “New Low Power and Fast SEC-DAEC and SEC-DAEC-TAEC Codes for Memories in Space Application” Integration, the VLSI Journal, (**SCIE**, **IF=1.345**, **Q3**), vol. 92, pp. 35-37, Sept. 2023. ISSN-0167-9260, **DOI**: 10.1016/j.vlsi.2023.04.004.
- [29] Heranmoy Maity, Mousam Chatterjee, Susmita Biswas, Aritra Bhowmik, Bineet Kaur, Ashish Kumar Singh, Parna Kundu Jagannath Samanta, A New Approach to Design of Cost-Efficient Reversible Quantum Dual-Full Adder and Subtractor, International Journal of Mathematical, Engineering and Management Sciences, (Scopus, IF:1.4, Q3), Vol. 9, No. 2, ISSN: 2455-7749, 341-351, Jan, 2024. **DOI**: 10.33889/IJMEMS.2024.9.2.018
- [30] Tapan Maity, Samaresh Paul, Jagannath Samanta and Prabir Saha, Design And Development of IoT-Based Smarttech-Agri Devices for Smart Agriculture Crop Field, Journal of The Institution of Engineers (India): Series B, Springer, January 2024, ISSN: 2250-2114, **DOI** : 10.1007/s40031-024-01002-5. (**Scopus**, **IF:0.237**, **Q3**).
- [31] Sudipta Bardhan, Manodipan Sahoo, Hafizur Rahaman and Jagannath Samanta, A Quasi-Ballistic Model for Short Channel Monolayer Graphene Field Effect Transistor Including Scattering Effects, IETE Journal of Research, (**SCIE**, **IF: 1.5**, **Q2**), ISSN: 0377-2063. Vol. 70, No. 9, April, 2024. **DOI**: 10.1080/03772063.2024.2352154. September 2024.
- [32] Dibyendu Chowdhury, Suddhendu DasMahapatra, Bishnu Prasad De, Madhusudan Maiti, Rajib Kar, Durbadal Mandal, Jagannath Samanta, Optimized Gate Metal Variant Structure for Graded-Channel (GC) Gate-Stack (GS) Double-Gate (DG) MOSFET to Enhance Switching Speed, Analog and RF Performance. Journal of Electronic Materials (Springer), (**SCIE**, **IF: 2.2**, **Q3**), ISSN: 1543-186X, vol:xx, no.xx, pp:1-14, Oct. 2024. **DOI**: 10.1007/s11664-024-11548-1.
- [33] Tapan Maity, Adi Nath Bhawani, Jagannath Samanta, Prabir Saha, Shubhankar Majumdar, Gautam Srivastava, MLSFDD: Machine Learning-based smart fire detection device for precision agriculture, IEEE Sensor Journal, (**Accepted**), (**SCIE**, **IF=4.3**, **Q1**), 16-12-2024. **DOI**: 10.1109/JSEN.2025.3525546

Communicated:

- [34] Tapan Maity, Ashok Mondal, Jagannath Samanta, Prabir Saha, IoT-based Soil Moisture Prediction Model (ISMPM) Using Multiple Linear Regression Algorithm For Smart Farming, IEEE Sensor Journal, (Under Review), Jan 2025.
- [35] Sourav Kumar Das, Raj Kumar Maity, Jagannath Samanta, PDEPE: CMOS Implementation of Power and Delay Efficient Polar Encoder for 5G Mobile Communication System, submitted in Springer.
- [36] Raj Kumar Maity, Akinchan Das, Jagannath Samanta, And Jaydeb Bhaumik, Improved ABER Performance of FSO Communication Systems with Soft Decision Decoding of TAEC Code, EURASIP Journal on Wireless Communications and Networking (SCIE)
- [37] Tapan Maity, Ashok Mondal, Jagannath Samanta, Prabir Saha, Shubhankar Majumdar, Gautam Srivastava, A Unique Soil Nutrients Prediction Method Based on Multiple Linear Regression - GradientDescent Algorithm for Precision Agriculture, IEEE Sensor Journal
- [38] Tapan Maity, Jagannath Samanta, Ashoke Mondal, and Prabir Saha, Monitoring of Soil Organic Matter (SOM) Using Near InfraRed spectroscopy (NIR) Sensor, communicated

B. Books and Book Chapters:

Books: 1. **J. Samanta**, A. K. Singh, “**An improved MOSFET I-V model and its application in nano-CMOS circuits**” Lap Lambert Academic Publishing, Germany, ISBN-978-3-659-44752-5, August-2013. Pages:72.

<https://www.lap-publishing.com/catalog/details/store/it/book/978-3-659-44752-5/an-improved-mosfet-i-v-model-and-its-application-in-nano-cmos-circuits?>

2. **Jagannath Samanta**, “**UDSM CMOS Circuits: Delay and Power Models**” Lap Lambert Academic Publishing, Germany, ISBN-978-3-659-52303-8, February-2014. Pages:97.

<https://www.lap-publishing.com/catalog/details/store/us/book/978-3-659-52303-8/udsm-cmos-circuits?>

Book Editorship:

1. Dr. Biplab Sikdar, Dr. Santi Prasad Maity, **Dr. Jagannath Samanta** (Corresponding Editor), Dr. Avisankar Roy, Proceedings of the 3rd International Conference on Communication, Devices and Computing - ICCDC 2021, Lecture Notes in Electrical Engineering, Springer Nature Singapore Pte Ltd. Vol: 851, ISBN: 978-981-16-9153-9, pages: 767. July 2021, DOI: 10.1007/978-981-16-9154-6

2. Dr. Dilip Kumar Sarkar, Dr. Pradip Kumar Sadhu, Dr. Sunandan Bhunia, **Dr. Jagannath Samanta** (Corresponding Editor), Dr. Suman Paul, Proceedings of the 4th International Conference on Communication, Devices and Computing - ICCDC 2023, Lecture Notes in Electrical Engineering, Springer Nature Singapore Pvt Ltd. Vol: 1046, ISBN: 978-981-99-2710-4, pages:709. August 2023, DOI: 10.1007/978-981-99-2710-4.

3. Dr. Chanchal Kumar De, Dr. Jyoti Prasad Bandyopadhyay, **Dr. Jagannath Samanta**, Dr. Banibrata Bag, Dr. Avisek Das, Dr. Sudipta Bardhan, Proceedings of 1st National Symposium on IoT and Cloud Computing (NSIC 2025), Published in Special Issue in Int. J. of HIT Transaction on ECON, Vol. 10, ISSN: 0973-6875, pp. 124, Jan 2025.

Book Chapters:

- [1] Rituparna Dasgupta, Dipankar Saha, **Jagannath Samanta**, Sayan Chatterjee, Chandan Kumar Sarkar, “*Implementation of a New Offset Generator Block for the Low-Voltage, Low-Power Self Biased Threshold Voltage Extractor Circuit*”, VDAT 2012, Progress in VLSI Design and Test, pp:156-165 (Published by **SpringerLink**, Lecture Notes in Computer Science, July-2012, Volume 7373/2012, 156-165, ISBN: 978-3-642-31494-0, DOI:10.1007%2F978-3-642-31494-0_18
- [2] **Jagannath Samanta**, Jaydeb Bhaumik & Soma Barman, “Compact RS(32, 28) encoder” Proc. of 1st Int. Conf. Intelligent Computing & Applications (ICICA 2014), NIT DGP, (Published by **SpringerLink**, Advances in Intelligent Systems and Computing vol.-343, ch.-10, Feb 2015, pp. 89-95.) (**Paper Presented**). ISBN: 978-81-322-2268-2, DOI:10.1007/978-81-322-2268-2_10
- [3] Jagannath Samanta, Jaydeb Bhaumik, Soma Barman and Raj Kumar Maity, “Binary error correcting codes for DNA databank,” Proc. in Int. Conf. on Communication, Devices and Computing (ICCDC2017), (Lecture Notes in Electrical Engineering (LNEE), Springer Nature Singapore Pte Ltd). (**Paper Presented**), Vol.470, pp.1-12, Nov. 2017. DOI:10.1007/978-981-10-8585-7_1.
- [4] Arghyadeep Sarkar, Jagannath Samanta, Amartya Barman and Jaydeb Bhaumik, “FPGA Implementation of OLS (32, 16) Code and OLS (36, 20) Code”, Proc. in Int. Conf. on Communication, Devices and Computing (ICCDC2017), (Lecture Notes in Electrical Engineering (LNEE), Springer Nature Singapore Pte Ltd). Vol.470, pp.69-81, Nov. 2017. DOI:10.1007/978-981-10-8585-7_7.
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- [6] Sayan Tripathi, Jhila Jana, Jagannath Samanta, Amandeep Anand, Chandrabhan Kumar, and Gautam Raj, FPGA and ASIC Implementation of SEC-DED-DAEC Codes for SRAM Application, Proceedings of the 2nd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 602. Springer, Singapore, March, 2019, pp.237-248, DOI:10.1007/978-981-15-0829-5_24.
- [7] Sayan Tripathi, Jhila Jana, Jagannath Samanta, Aman Raj, Deep Ranjan, and Mayank Pratap Singh, Design and Evaluation of Neale Based Multi-bit Adjacent Error Correcting Codec for SRAM, Proceedings of the 2nd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 602. Springer, Singapore, 2019, pp.259-268, (Best paper award), DOI:10.1007/978-981-15-0829-5_26.
- [8] Sayan Tripathi, Jhila Jana, Jagannath Samanta, and Suvam Barui, Modern Smart Classroom based Touch Technology using Digital Image Processing, Proceedings of the 2nd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 602. Springer, Singapore, 2019, pp.515-524, DOI:10.1007/978-981-15-0829-5_50.
- [9] Raj Kumar Maity, Jagannath Samanta, and Jaydeb Bhaumik, New Compact SEC-DED-DAEC Code for Memory Applications, Proceedings of the 2nd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical

- Engineering, vol 602. Springer, Singapore, 2019, pp.321-330, (Best paper award), 10.1007/978-981-15-0829-5_32.
- [10] Akash Adhikary, Rishav Vatsa, Aman Burnwal and Jagannath Samanta, Performance Evaluation of Low-Cost RGB-Depth Camera and Ultra-Sonic Sensor, Proceedings of the 2nd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 602. Springer, Singapore, 2019, pp.331-342, 10.1007/978-981-15-0829-5_33.
 - [11] Jhilam Jana, Sayan Tripathi, **Jagannath Samanta**, Jaydeb Bhaumik and Soma Barman, An Approach to Reduce Power Consumption and Delay of Single Error Correction Codes in WSN for IoT Applications, In: Das N.R., Sarkar S. (eds) Computers and Devices for Communication. CODEC 2019. Lecture Notes in Networks and Systems, vol 147. Springer, Singapore. pp. 193-203, DOI: 978-981-15-8366-7_27.
 - [12] Raj Kumar Maity, Jagannath Samanta and Jaydeb Bhaumik, FPGA-based Low Delay Adjacent Triple-bit Error Correcting Codec, Proceedings of the **ICIA-2020**, NIT Jamshedpur, Lecture Notes in Electrical Engineering. vol 825. Springer, Singapore, December 2020, ISBN: 978-981-16-7637-6, pp. 419-429, DOI: 10.1007/978-981-16-7637-6-37.
 - [13] Jagannath Samanta, Raj Kumar Maity, Debnath Ghosh, and Sudipta Bardhan, Performance Analysis of Barlekamp-Massey based KES block for 3-Byte RS Decoder, Proceedings of the 3rd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 851. Springer, Singapore, August, 2021, pp. 15-24, DOI: 10.1007/978-981-16-9154-6_2
 - [14] Raj Kumar Maity, Jagannath Samanta, and Jaydeb Bhaumik, An Efficient Decoding of SEC-DED-DAEC Code with Odd-Column-Weight H-matrix, Proceedings of the 3rd International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 851, Springer, Singapore, August, 2021, pp. 689-698, DOI: 10.1007/978-981-16-9154-6_63.
 - [15] Tapan Maity, Pranabendu Giri, Rohit Sasmal, Niladri Biswas, Sourav Das, Raj Kumar Maity, Prabir Saha, Jagannath Samanta, Design of Smart IoT-Based Gas Leakage Detection and Prevention Devices for Hydrogen Station, Proceedings of the 4th International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 1046, Springer, Singapore, March, 2023, pp. 531-545, 10.1007/978-981-99-2710-4_43
 - [16] Sweta Bijali Maity, Raj Kumar Maity, Jagannath Samanta, Chanchal Kumar De, An Efficient SEC-DCEC Code for Protecting Data Bits in IoT Devices, Proceedings of the 4th International Conference on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 1045, Springer, Singapore, March, 2023, pp. 391-400, DOI: 10.1007/978-981-99-2710-4_32. Published July 2023.
 - [17] Tapan Maity, Ayush Roy, Oisik Das, Rakshat Kashyap, Anjan Mishra, Jagannath Samanta, Design and Development of IoT-Based Smart Health Monitoring System for Greenhouse Cultivation, Proceedings of ICTDsC 2023, Siliguri, Studies in Autonomic, Data-driven and Industrial Computing (SADIC), March 2023, pp. 173-185, DOI:10.1007/978-981-99-5435-3_12. Published Jan 2024.
 - [18] Raj Kumar Maity, Akinchan Das, Jagannath Samanta, and Jaydeb Bhaumik, "The Combined ECC Scheme with Outer 3-bit BEC and Inner SEC-DAEC Codes for FSO Communication System", Proceedings of Third International Conference on Advanced Computing and Applications, ICACA 2024, Techno India, Kolkata,

- "Lecture Notes in Networks and Systems" Springer, Feb 2024. ISBN: 978-981-97-4799-3, pp:1-15, Nov 2024. DOI:10.1007/978-981-97-4799-3_5.
- [19] Adarsh Kumar, Sneha Basak, Jagannath Samanta, Raj Kumar Maity, An IoT-based Smart Hybrid Power Management System with Accurate Forecasting and Load Strategy, Proceedings of the 7th Int. Conf. on Energy Systems Drive and Automation (ESDA2024, Lecture Notes in Electrical Engineering, vol xxx, Springer, Singapore, April, 2025, pp. xxx, DOI:. Published July 2025 (Paper presented)

C. Conference Papers:

International Conference:

- [1] **J Samanta** and B P De, "Comprehensive analysis of delay in UDSM CMOS circuits", Proceeding of, ICECCT'11, Villupuram, Tamil Nadu, India, **IEEE explore**, ISBN:978-1-4577-1894-6/11, 15-17, Nov-2011, pp:29-32. **(Paper Presented)**
DOI: 10.1109/ICECCT.2011.6077064
- [2] **J Samanta** and B P De, "Delay analysis of UDSM CMOS VLSI circuits", International Conference ICCSTD-2011, Kerala, Procedia Engineering, Volume 30, 2012, **(Science Direct)** March-2012, pp:135-142. **(Paper Presented)**, DOI::10.1016/j.proeng.2012.01.844,
<http://www.sciencedirect.com/science/article/pii/S1877705812008545>
- [3] Ashish Kumar Singh & **Jagannath Samanta**, "Different Physical Effects in UDSM MOSFET for Delay & Power Estimation: A Review", International Conference on Electrical, Electronics and Computer Science (SCEECS-2012), NIT Bhopal, ISBN-978-1-4673-1515-9/**IEEE Explore**, March-2012, pp:1-5.
DOI: 10.1109/SCEECS.2012.6184747
<http://ieeexplore.ieee.org/document/6184747/>
- [4] Ashish Kumar Singh, **Jagannath Samanta** & Jaydeb Bhaumik, "Modified I-V Model for Delay Analysis of UDSM CMOS Circuits", International Conference on Communications, Devices and Intelligent Systems (CODIS), Jadavpur University, 978-1-4673-4700-6/12, **IEEE Explore**, Dec-2012, pp:369-372. **(Paper Presented)**
DOI: 10.1109/CODIS.2012.6422212,
<http://ieeexplore.ieee.org/document/6422212/>
- [5] **Jagannath Samanta**, Razia Sultana & Jaydeb Bhaumik, "FPGA Based Modified Karatsuba Multiplier" International Conf. on VLSI and Signal Processing (ICVSP14-**IEEE Sponsored**) at IIT KGP, Jan. 2014, pp:1-6.**(Paper Presented)**.
- [6] **Jagannath Samanta**, Jaydeb Bhaumik & Soma Barman, "Low Complexity 3-Symbol Error Detecting RS(23, 17) Code". 3rd Int. Conf. on Computing, Communication and Sensor Network, (CCSN2014), PIET, Odshia, ISBN No.:81-85824-46-0, pp:30-37, Dec-2014, **(Paper Presented)**.
- [7] **Jagannath Samanta**, Jaydeb Bhaumik & Soma Barman, "Area Optimized SEC-DED Codec for Computer Memory," Proc. 5th Int. Conf. on Computing, Communication and Sensor Network, (CCSN2016), Kolkata, ISBN No.:81-85824-46-0, pp:159-163, Dec. 2016, **(Paper Presented)**.
- [8] Raj Kumar Maity, **Jagannath Samanta**, and Jaydeb Bhaumik, An Area and Power Efficient Double Adjacent Error Correcting Parallel Decoder based on (24, 12) Extended Golay Code, Proc. In IEEE ICECCT19, Coimbatore, Feb. 2019. **IEEE Explore**, DOI: 10.1109/ICECCT.2019.8869098.

- [9] Sayan Tripathi, Jhila Jana, Jagannath Samanta, and Jaydeb Bhaumik, Fast and Power Efficient SEC-DED and SEC-DED-DAEC Codes in IoT based Wireless Sensor Networks, IEEE Region 10 Conference (TENCON-2019), Oct. 2019, pp.540-545, 10.1109/TENCON.2019.8929354.
- [10] Raj Kumar Maity, Sayan Tripathi, **Jagannath Samanta**, and Jaydeb Bhaumik, Compact SEC-DED-DAEC and SEC-DED-TAEC Decoder for SRAMs, Proc. 8th Int. Conf. on Computing, Communication and Sensor Network, (CCSN2019), Hyderabad, ISBN No.:81-85824-5, vol. 1, pp:42-47, Oct. 2019, **(Paper Presented)**.
- [11] Raj Kumar Maity, **Jagannath Samanta**, and Jaydeb Bhaumik, An Improved SEC-DED-DAEC Code for SRAMs, 4th Int. Conf. on 'Energy Systems, Drives and Automations', ESDA2021, Dec-2021. pp. 19.
- [12] Srikant Kumar Beura, **Jagannath Samanta**, Bishnulatpam Pushpa Devi, Prabir Saha, Floating Point Adder using Inexact Mantissa Adder, 4th International Conference on Computing and Communication Systems (I3CS), IEEE Explore, March 2023, ISBN:979-8-3503-2377-1, DOI: 10.1109/I3CS58314.2023.10127550.
- [13] Tapan Maity, Adi Nath Bhawani, Jagannath Samanta and Prabir Saha, Design of Smart Protective Devices For Precision Agriculture Using Internet-of-Things, 6th Int. Conf. on 'Energy Systems, Drives and Automations', ESDA2023, Dec-2023.
- [14] Pritam jana, **Jagannath Samanta**, Tapan Maity, Design and Implementation of an Efficient Arduino-Based Smart Home Automation System, Proceedings of 1st National Symposium on IoT and Cloud Computing (NSIC 2025), Published in Special Issue in Int. J. of HIT Transaction on ECON, Vol. 10, ISSN: 0973-6875, pp. 7-14, Jan 2025, DOI: 10.5281/zenodo.14591143.
- [15] Suprotim Chatterjee, Arunava Maity, **Jagannath Samanta**, Design Of Smart Accident Detection And Prevention System Using IoT Technology, Proceedings of 1st National Symposium on IoT and Cloud Computing (NSIC 2025), Published in Special Issue in Int. J. of HIT Transaction on ECON, Vol. 10, ISSN: 0973-6875, pp. 24-34, Jan 2025, DOI: 10.5281/zenodo.14591287.
- [16] Md Samim Bari, Md Ashhad Raza, Ravi Kumar, Suraj Kumar Gupta, Susmit Kumar Shaw, Wasibul Hossain, **Jagannath Samanta**, Soumya Mukherjee, Design and Web Framework of Secure Electronic Voting System, Proceedings of 1st National Symposium on IoT and Cloud Computing (NSIC 2025), Published in Special Issue in Int. J. of HIT Transaction on ECON, Vol. 10, ISSN: 0973-6875, pp. 73-79, Jan 2025, DOI: 10.5281/zenodo.14591852.
- [17] Anirban Roy Chowdhury, **Jagannath Samanta**, Tapan Maity, and Sampa Samanta, Design And Development Of Smart Iot-Based Air Quality Detection And Monitoring Devices For Industry 4.0, Proceedings of 1st National Symposium on IoT and Cloud Computing (NSIC 2025), Published in Special Issue in Int. J. of HIT Transaction on ECON, Vol. 10, ISSN: 0973-6875, pp. 39-43, Jan 2025, DOI: 10.5281/zenodo.14591383.

National Conference:

- [1] **J. Samanta**, B. P. De, B. Bag & R. K. Maity, “Comparative study for delay & power dissipation of CMOS Inverter in UDSM range” Proc. of the National Conference on Advanced Communication Systems and Design Techniques, NCACD 2011, HIT, Haldia, November-2011, pp:70-74. **(Paper Presented)**

- [2] R. K. Maity, **J. Samanta**, “Construction and performance studies of a pseudo-orthogonal code for fiber optic CDMA LAN” Proc. of the National Conference on Advanced Communication Systems and Design Techniques, NCACD 2011, HIT, Haldia, November-2011, pp:123-126.
- [3] **Jagannath Samanta**, Mousam Halder and Bishnu Prasad De, “Design and Analysis of high speed low power Carry Look-Ahead Adder using static logic” Proc. of the National Conference on Advanced Communication Systems and Design Techniques, NCACD 2012, HIT, Haldia, September-2012, pp:79-83. **(Paper Presented)**.
- [4] Jaydeb Bhaumik, Anindya Sundar Das and **Jagannath Samanta**, “Architecture for Programmable Generator Polynomial Based Reed-Solomon Encoder and Decoder” Proc. of the National Conference on Advanced Communication Systems and Design Techniques, NCACD 2012, HIT, Haldia, September-2012, pp: 87-90.

Seminar Publication:

- [1] S Paul, D. Mallick, **J. Samanta**, S. Ojha & A. K. Jana, “Explosive Detection with Electronic Nose”, National Seminar on Explosive Detection, Dept. of ECE, Haldia Institute of Technology under TEQIP on May 19, 2007, pp:41-42.
- [2] S. Paul, D. Mallick, **J. Samanta**, S. Chottopadhyay and S. Khanra, “Explosive Detection with THZ Frequency”, National Seminar on Explosive Detection, Dept of ECE, Haldia Institute of Technology under TEQIP on May 19, 2007, pp: 43-45.
- [3] S Mal, S Sarkar, S Mondal, B P De, **J. Samanta**, P Satpathy and B Bag, “Design & Development of Array Multiplier for VLSI Applications Using SPICE Simulation Tool”, Proceeding of National Conference at Garbeta college, Jan2012, pp:90-95.

INVITED TALKS:

1. “Introduction to CMOS VLSI Design” on 6th Sep. 2008 at MCKV College of engineering, Howrah.
2. “Performance Analysis of Error Correcting Codes for Stored DNA Sequences”, organized by Dept. of Mathematics, Mahadevananda Mahavidyalaya, Barackpur, Kolkata on 04-01-2024.
3. “VLSI Implementation of Reed Solomon (RS) Codec for UWB Applications”, organized by Dept. of Mathematics, Mahadevananda Mahavidyalaya, Barackpur, Kolkata during on 13 Feb. 2024.
4. “National Education Policy-2020” organized by Academic Staff Development Centre under IQAC, Haldia Institute of Technology, on 19-04-2024.
5. “Design of Cellular Automata based Non-Binary Error Correcting Codes”, organized by Dept. of Mathematics, Mahadevananda Mahavidyalaya, Barackpur, Kolkata on 24-06-2024.

EXTERNAL EXAMINER/EXPERT:

Sl. No.	Name of Exam	Conducted by Board / University	Date/ Duration	Role
1	Odd Semester Exam	West Bengal University of Technology, Kolkata	Dec. 2010	University Station Supervisor
2	M.Tech Project Evaluation	ECE, ITME, 24 Pargans (S)	01/12/2011	External examiner
3	Odd Sem Exam	ECE, ITME, 24 Pargans (S)	28-11-2013	B.Tech laboratory

				external examiner
4	WBJEE14	WBJEEB	19-20, April, 2014	Board Observer
5	Odd Sem Exam	IRPE, Calcutta University	Nov-2014	B.Tech laboratory external examiner
6	Even Sem Exam	IRPE, Calcutta University	16.05.2015	B.Tech laboratory external examiner
7	Odd Sem Exam	IRPE, Calcutta University	29.11.2016	B.Tech laboratory external examiner
8	Odd Sem Exam	IRPE, Calcutta University	16.12.2016	B.Tech laboratory external examiner
9	D.El.ED exam	NIOS (MHRD, GOI)	3 rd Feb, 2019	Special observer
10	WBJEE19	WBJEEB	26 th May, 2019	Board Observer
11	JENPAS (UG) 19	WBJEEB	30 th June, 2019	Board Observer
12	JECA19	WBJEEB	13 th July, 2019	Board Observer
13	HS(10+2) exam	NIOS (MHRD, GOI)	14-16 and 24 th October, 2019	Special Observer
14	D.El.ED supplementary exam	NIOS (MHRD, GOI)	17-18, Jan, 2020	Special Observer
15	WBJEE-20	WBJEEB	2 nd Feb, 2020	Board Observer
16	WBJEE-21	WBJEEB	17 th July, 2021	Board Observer
17	JENPAS (UG) 21	WBJEEB	31 th July, 2021	Board Observer
18	ANM (R) & GNM 21	WBJEEB	22 nd Aug, 2021	Board Observer
19	SMFWBEE 2021	State Medical Faculty of West Bengal	3 rd Oct, 2021	Observer
20	Winter Exam	IGNOU	March 2022	Invigilator
21	JENPAS (UG) 22	WBJEEB	15 th May, 2022.	Board Observer
22	SMFWBEE 2022	State Medical Faculty of West Bengal	24 th July 2022	Observer
23	WBJEE-23	WBJEEB	30 th April, 2023	Board Observer
24	NEET (UG) 2023	NTA	7 th May, 2023	Observer
25	WBJEE-24	WBJEEB	28 th April, 2024	Board Observer
26	NEET (UG) 2024	NTA	5 th May, 2024	Observer
27	JENPAS (UG) 2024	WBJEEB	30 th June, 2024	Board Observer
28	UGC NET 2024	NTA	21-01-25 and 27-01-25	Observer
29	Question Moderator	Swami Vivekanda University	28-Jan-2025	Moderator

STUDENT THESIS GUIDED:

i. B.Tech Thesis Guided:

Sl No.	Name of the project	Name of students	Date of awarded	Remarks
1.	Design and power performance optimization of Memory using dual	Abhishek Gupta, Rahin Biswas	16.04.2009	Internal guide

	bit CAM cells			(JU)
2.	An improved design of synchronous up/down counters with VLSI Technologies	Arnab Roy, Dipanjan Pradhan	16.04.2009	Internal guide (JU)
3.	Temperature Sensor	Rakesh Ranjan, Kumar Sundaram, Pankaj Kumar Prasad, Nishant Kumar	07.05.2010	
4.	Mobile cell phone charger	Manish Kumar, Rahul Kumar, Uttam Kumar, Pradeep Kumar	07.05.2010	
5.	Design & Construction of remote control fan regulator	Chayan Kr. Dutta, Arpan Jana, Amit Dasgupta, Argha Das	07.05.2010	
6.	Design and implementation of high speed Carry look ahead adder	Rachaita Chaklader, Lipika Barai, Bhaswati Sarkar	11.04.2011	
7.	Design and implementation of 4 bit ALU	Souvik Bera, Sovona Jana, Subrajit Majumder, Supriyo Mondal	11.04.2011	
8.	Analysis and Comparison of different topologies of Full Adder circuits in Submicron Technology	Anurag Mondal, Richa Rashmi, Ishika Kundu, Ritubritta Koley, Diwakar Mishra, Swesh Kumar	09.05.2012	
9	Performance Analysis of Carry Select Adder Using EDA Simulation Tool	Brijita Santra, Madhurima Saha, Moitri Sutradhar, Moumita Basak	10.05.2013	
10	Performance Comparison of Combinational Circuits Using Static And Dynamic Logic	Tanushri Banerjee, Mampi Bera, Sejuti Gupta, Rituparna Mandal	24.04.2014	
11	Design Of Reed Solomon (255, 243) Encoder And Decoder Using Verilog	Ritesh Kumar, Rajni Kant Pandey, Sucheta Biswas, Somnath Das	11.05.2015	
12	FPGA and ASIC based implementation of single error correcting codec for DNA bases	Anunay Kumar, Raja Babu, Piyali Chakraborty, Vikash Kumar, Saptarshi Baisya	03.06.2016	
13	Design and Implementation of SEC-DED Codec for Memory Applications	Akash Kewat, Megha Bhardwaj, Pawan Kumar, Pallavi Kumari	01.06.2017	
14	Design and Implementation of triple error correcting (15, 5) BCH code	Sumit Agarwal, Sruti Priya, Sarabjit Singh	01.06.2017	
15	Design and Implementation of OLS code	Arghayadeep Sarkar (Jalpaiguri Govt. College)	01.06.2017	
16	FPGA AND ASIC based implementation of Dutta multi-bit error correcting codes	Chandrabhan Kumar, Gautam Raj, Amandeep Anand	04.05.2018	
17	Design and Implementation of Neale based Multi-bit Adjacent Error Correcting Codec	Aman Raj, Mayank Pratap Singh, Deep Ranjan	04.05.2018	
18	Design and Development of an	Akash Adhikary, Amit Kumar,	23.05.2019	

	Automatic Parachute Control System for Civilian and Military Applications	Nitish Tiwary, Harsh Raj		
19	Error correction codes in Wireless Sensor Network	Sumit Sagar, Shubham Kumar, Shashi Bhusan Kumar, Sandeep Tudu	July, 2020	
20	Fault Tolerant Wireless Sensor Network	Yasvant Agarwal, Souvik Sen, Sourav Mishra, Rishika Roy	July, 2021	
21	Fault tolerant DNA based digital storage system	Ranjan Kumar, Sonu Kumar, Satyam Kumar, Saurabh Kumar Jha	July, 2021	
22	House Price Prediction Using Linear Regression	Sourav Kumar, Semanto Saini, Rishav Swaroop, Nishant Kumar	June, 2022	
23	Design and Development of e-Polling Web Application	Md Samim Bari, Md Ashhad Raza, Ravi Kumar, Susmit Kumar Shaw, Suraj Kumar Gupta	June, 2022	
24	Measurement and monitoring of IoT based smart precision farming	Ayush Roy, Oisik Das, Rakshat Kashyap, Raju Kumar, and Medha Chakraborty	June, 2023	
25	IoT-Based Milk Adulteration Detection and Monitoring Techniques	Rajat Ganguly, Ramit Podder, Priya Singh, Rashika Rajeev and Ritik Sinha	June, 2023	
26	FPGA Implementation of LDPC Code for Adjacent Error Detection in Nanometer Devices	Adarsh Kumar, Debalina Chakraborty, Devashree Manna, Dibakar Bera, Satirtha Chatterjee	June, 2024	

ii. M.Tech Thesis Guided:

Sl No.	Name of the project	Name of students	Date of awarded	Remarks (Co-guide)
1.	Comparison of CNT & Copper interconnects and its applicability of CNT as future interconnects	Sandip Bhattacharya	29.04.2011	Dr. Debaprasad Das, MSIT Kolkata
2.	Modeling of CNT FET in Verilog – AMS & applicability in future microelectronics circuits.	Subhajit Das	29.04.2011	Dr. Debaprasad Das, MSIT Kolkata
3.	Comparative Study Of High Speed Carry Look Ahead Adder Using Different Logic Styles	Mousam Halder	21.05.2012	
4.	A simple & accurate MOSFET I-V model and its application for delay analysis in Nano-CMOS circuits	Asish Kumar Sinha	21.05.2012	
5.	Design and Implementation of Low-Voltage, Low-Power Self-Biased CMOS Threshold Voltage Extractor circuit	Rituparna Dasgupta	21.05.2012	Dr. Sayan Chatterjee, (JU)

6	Performance Analysis Of a Modified Karatsuba Multiplier And Its Application In Circular Convolution	Razia Sultana	20.05.2013	
7	Performance Analysis Of Different Combinational Circuits Using Modified GDI Techniques	Debrupa Metia	16.05.2014	
8	Design And Implementation of Double Byte Reed Solomon Encoder Using 45nm Technology	Madhuresh Suman	25.05.2015	Mr. Dibyendu Chowdhury
9	FPGA Implementation of RS(255, 223) codec for deep space communication	Arunabha Patra, CU	25.05.2015	
10	Design and implementation of RS(255, 223) encoder and decoder in FPGA	Bappaditya Kuila	25.05.2015	
11	Design and implementation of RS(47, 41) codec for intelligent home networking	Neha Chauhan	13.06.2016	
12	Design and implementation of RS(255, 249) codec for DNA sequencing	Mandira Sahoo	13.06.2016	
13	Area and Delay efficient SEC-DED-DAEC codes for SRAM Memory	Sayan Tripathy	04.06.2018	
14.	Soft Error Analysis of TCAM Devices for Network Applications	Debnath Ghosh	30.08.2021	
15.	Design And Implementation of SEC Based Orthogonal Latin Square (OLS) Code for Cache Memory	Saptarshi Mondal	30.06.2024	
16.	GF Parallel Multiplier	Md. Wasibul Hossain	30.06.2025	

iii) Ph.D. Thesis Guidance:

Sl No.	Name of the Topic	Name of student	University	Role	Status
1.	Design and Implementation of Error Correcting Codes for Storage and Communication Systems	Mr. Raj Kumar Maity	Dept. of ETCE, Jadavpur University, Kolkata	Co-supervisor with Dr. Jaydeb Bhaumik, Professor, ETCE, JU, Kolkata	18.06.2019 (Registered) Thesis submitted on 09-09-2024
2.	Design of Error-Tolerant Smart Devices for Emerging Application using Machine Learning	Mr. Tapan Maity	NIT Meghalaya	Co-Supervisor with Dr. Prabir Saha, HOD, ECE, NIT, Meghalaya	Enrolled, P23EC005, 31-07-2023 Registered 20-09-2024
3.	Design and Implementation of Efficient Smart Channel Encoders and Decoders Circuits for Emerging Applications	Mr. Sourav Das	MAKAUT, West Bengal	As Supervisor	Preparing for Enrolment

iv) Research Grant Received:

Sl. No.	Title of project	Fund Amount (Rs.)	Funding Agency, ID No.	My Role	Co-Investigator Name
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1	Smart Measurement and Monitoring of Agricultural Soil using Cloud IOT and Android System	10,003/-	(Seed Fund) Haldia Institute of Technology, Haldia	Principal Investigator (29-12-21 to 30-06-22)	Mr. Tapan Maity
2	Design and development of a Low Cost Compact Multipurpose Eco-refrigerator	21,150/-	(Seed Fund) Haldia Institute of Technology, Haldia	Principal Investigator (07-04-22 to 01-07-22)	Mr. Sayan Dutta
3	Design and development of IOT-based smart devices to measure air and soil condition in agriculture fields	20,000/-	Project ID: UG2023007, IEI R&D Grant-in-aid Scheme.	Principal Investigator (Jun 22-Jan 23)	Mr. Tapan Maity, Mr. Ayus Roy, Mr. Oisik Das
4	Design and development of IoT-based Smart Air Quality Monitoring System	10,000/-	(Seed Fund) Haldia Institute of Technology, Haldia	Principal Investigator (July 23-Jun 23)	Mr. Tapan Maity
5	Design and development of smart IoT-based air quality detection and monitoring devices for Industry4.0	22,000/-	Project ID: UG2023024, IEI R&D Grant-in-aid Scheme.	Principal Investigator (25 th May, 23-March 24)	Mr. Tapan Maity, Deblina Chakraborty, Anirban Roy Choudhury
6	Soil Nutrient Analysis Using Machine Learning Techniques for Precision Agriculture	10,000/-	(Seed Fund) Haldia Institute of Technology, Haldia	Principal Investigator (July 24-June 24)	Mr. Tapan Maity
7	Smart Agriculture: AI-Driven Soil Parameter Monitoring for Organic Farming in Meghalaya	7,08,750/-	North East Centre for Technology Application & Reach (NECTAR), DST, Govt. of India	Co-Principal Investigator (Sept., 24-Aug. 25), 12 Months	PI-Dr. Prabir Saha, Associate Professor, Dept. of ECE, NIT Meghalaya
8	Financial Assistance for National Symposium on “IoT and Cloud-computing: Smart Solutions for Tomorrow”, NSIC2025	1,70,000/-	Science & Engineering Research Board (SERB) Seminar/Symposium a Scheme-ANRF)	Principal Investigator (9-10, January, 2025)	Convenor
9	Design And Development Of Smart Devices For Estimation Of Soil Characteristics Using Lora Technology In Precision Agriculture	13,300/-	(Seed Fund) Haldia Institute of Technology, Haldia	Principal Investigator (January 25-December 25)	Mr. Tapan Maity
10	Design And Development	45,000/-	R.5/2/PG/2024-	Principal	Mr. Tapan

	of Smart Devices for Estimation of Soil Characteristics Using Lora Technology In Precision Agriculture		25/PG2025009, IEI R&D Grant-in-aid Scheme.	Investigator (05-03-25 to 04-03-2026)	Maity, Pritam Jana
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v) Project Proposal accepted in Competition:

Sl. No.	Name of Proposal	Name of students	Details of event	Status	Role
1	Tryambaka-Autonomous mapping and surveillance system	Akash Adhikary Aman Burnwal Rishav Vatsa	DRDO Robotics and Unmanned Systems Exposition (DRUSE), 26-27th March, 2018, at Jadavpur University, Kolkata.	Qualified for zonal level and won Rs. 10000/- prize money.	Team Leader
2	eChakshu- An e-commerce website for visually impaired people	Mr. Aditya Prakash, Mr. Ankit Pairwar, Mr. Dipesh	4 th Regional Science and Technology Congress (Southern Region) 23-24th Dec, 2019, MAKAUT, West Bengal,	Qualified for presentation	Team Mentor

MAJOR SUBJECTS TAUGHT:

UG/PG Level	Theory	Practical
UG Level:	a) Basic Electronics, b) Digital Electronics, c) Analog Electronics, d) VLSI Circuits & Systems e) EDA for VLSI Design. f) Embedded System g) Information Theory and Coding h) Error Correcting Codes	a) Basic Electronics Lab, b) Digital Electronics Lab, c) VLSI Design Lab, d) Circuit Theory Lab. e) Analog Electronics Lab f) EDA for VLSI Design lab
PG Level	a) Microelectronics & VLSI, b) Digital IC Design c) VLSI Physical Design & Testing d) Architectural Design of Integrated Circuits	a) CAD Tools for VLSI design

PROFESSIONAL INVOLVEMENTS:

A. As a Reviewer:

i. Journals:

1. IEEE Transactions on Computers-No. 02
2. IEEE Transactions on VLSI System-No. 15
3. IEEE Transactions on Consumer Electronics- No. 01
4. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems-03
5. Cryptography and Communications (Springer)-No. 02
6. China Communication-02
7. World Applied Sciences Journal-01
8. Alexandria Engineering Journal-(Elsevier)-02

9. International Journal of Engineering and Technology Innovation-01
10. Computers and Electrical Engineering, (Elsevier)-02
11. Journal of Current Science and Technology (Scopus indexed)-01
12. Cybernetics and Systems-01
13. Journal of Supercomputing (Springer)-01
14. Applied Artificial Intelligence (Springer)-01
15. Journal of the Institution of Engineers (India): Series B (Springer)-01
16. Journal of Engineering Research(Scopus, Elsevier)-01
17. IEEE Transactions on Information Forensics and Security-01
18. Integration, Elsevier-02
19. IEEE Transactions on Magnetics-01
20. IEEE Transactions on Geoscience and Remote Sensing-01
21. IETE Journal of Research
22. Journal of System Architecture
23. ACM Transactions on Embedded Computing Systems
24. IEEE Access

ii. Conferences:

1. NCACD 2011, HIT, Haldia-06
2. NCACD 2012, HIT, Haldia-07
3. ICICA 2014, NIT DGP-02
4. CECNet2014, Shanghai, China-02
5. ICCDC2017, HIT, Haldia-07
6. SNSP2018, China-01
7. ICCDC2019, HIT, Haldia-07
8. CCSN 2019, IAE, Hyderabad, India-03
9. ESDA-2019, Kolkata-04
10. PASC21, University of Geneva, Geneva, Switzerland-01
11. MICRO 2021, Kolkata-03
12. ICCDC2021, HIT, Haldia-07
13. CCSN 2021, Kolkata, India-01
14. ESDA-2021, Kolkata-02
15. ISAI-2022, HIT, Haldia-02
16. MICRO 2022, University of Technology, Jaipur, Rajasthan-01
17. ICCDC 2023, HIT Haldia-05
18. ICTDsC 2023, SIT, Siliguri-02
19. ASPCON 2023, HIT, Haldia
20. CODEC 2023, IRPE, Calcutta University-04
21. ICACA 2024, Techno India University, Salt lake Kolkata

B. As a Session Chair:

- i. ICCDC 2019, HIT Haldia, March 14-15, 2019.
- ii. 2nd Int. Conf. on Energy Systems, Drives and Automations (ESDA2019), 28th-29th Dec. 2019, Celesta, VIP Road, Kolkata-700059.
- iii. National Conf. on Innovation in Sustainable Energy and Technology, ISET INDIA 2020 organized by Energy Institute, Bengaluru during 3-4, Dec, 2020.
- iv. 8th Int. Conf. on Microelectronics, Circuits & Systems, (MICRO 2021), 8th-9th May. 2021, Kolkata, West Bengal, Applied Computer Technology, Kolkata.

- v. 10th Int. Conference on Computing, Communication and Sensor Networks (CCSN2021), 2-4, Oct 2021, Applied Computer Technology, Kolkata & NIT Rourkela.
- vi. 4th Int. Conf. on Energy Systems, Drives and Automations (ESDA2021), 30th-31th Dec. 2021, Hotel The Maureen, VIP Road, Kolkata-700059. Applied Computer Technology, Kolkata & IEST, Shibpur, Howrah.
- vii. 7th Int. Conf. on Energy Systems, Drives and Automations (ESDA2024), 14th-15th Dec. 2024 organized by Dept of ECE, Dumka Engineering College, Dumka. Jharkhand.

C. Technical Program Committee Member:

- ii. The 3rd International Conference on Engineering Mathematics and Computing (ICEMC 2020) at CSE & SAS, HIT, Haldia, India, 5-7 February, 2020.
- iii. Conf. on IoT and its Applications (CIA-2020), 11-12 July 2020, CSE, NIT Jamshedpur.
- iv. Int. Symposium on Artificial Intelligence (ISAI-2022), February 17-19, 2022, HIT, Haldia, India.
- v. 1st Int. Conf. on Recent Trends in Science and Technology (ICRTST-2K22).
- vi. 1st International Conference on Innovations in Data Analytics (ICIDA 2022)
- vii. 2nd International Conference on Innovations in Data Analytics (ICIDA 2023).
- viii. 3rd International Conference on Innovations in Data Analytics (ICIDA 2024).
- ix. International Conference on Computational Intelligence and Information Retrieval (CIIR 2025) during 24th – 25th April 2025.

D. Journal Editorial Board Member:

- i. Senior Associate Editors, in International Journal of HIT Transaction on ECCN ISSN: 0973-6875.
- ii. Academia Materials Science

E. Membership:

- i. Member of “The Institution of Engineers (India)”, Membership number: M1591066, from August, 2017 to August, 2023.
- ii. Fellow of “The Institution of Engineers (India)”, Fellow number: F-1300152, from Sept. 2023 to till date.
- iii. Associate member of Universal Association of Computer and Electronics Engineers (UACEE) (Membership ID: AM10100052323). 2017
- iv. The Society of Digital Information and Wireless Communications (SWIC) (Membership ID: 11741) 2013
- v. International Association of Engineers (IAENG)- (Membership ID: 158527) 2014

ADMINISTRATIVE RESPONSIBILITIES:

- i. Worked as Departmental Post graduate student coordinator, July, 2015 to June, 2024
- ii. Worked as a member of Institute student welfare committee, July, 2014 to Nov. 2023
- iii. Worked as a member of Institute routine committee member, July, 2014 to June, 2016
- iv. Worked as a member of Institute cultural committee July, 2014 to Nov. 2023
- v. Worked as a member of departmental discipline committee, June, 2018 to till date

- vi. MAKAUT Exam supervisor, Jan, 2020 to July, 2022
- vii. Departmental In-charge in absence of HOD
- viii. Departmental committee members for MAKAUT, AICTE, NAAC, NBA accreditation
- ix. Convenor of “Departmental Academic Audit Committee”, July, 2016 to till date.
- x. Expert (as a Accreditation and observer, No. 5567) at National Institute of Electronics & Information Technology (NIELIT)
- xi. Reviewer/Moderator at AICTE, Student learning Assessment (SLA) Project, 2021.
- xii. Departmental Training & Placement In-charge, July, 2019 to June 2024
- xiii. OIC, MAKAUT, August, 2022 to till date
- xiv. OIC, HIT Autonomous, August, 2022 to till date
- xv. NEP Nodal Officer, October 2023 to till date
- xvi. Member of R&D Monitoring Committee Dec. 2023 to till date
- xvii. Member of Institutional Innovation Council (IIC), Dec. 2023 to till date
- xviii. Member of Entrepreneurship Development Cell (EDC), July, 2023 to till date
- xix. Convenor, Programme Assessment and Quality Improvement Committee (PAQIC), Sept 2022 to till date

ACHIEVEMENTS:

1. Top ranker upto class X.
2. Received Jindal Trust Studentship Scholarship from Sitaram Jindal Foudation during H.S. course (1998-2000).
3. Received Jindal Trust Studentship Scholarship from Sitaram Jindal Foudation during B.Tech course (2001-2005).
4. Received Gold Medel during M.Tech program (July, 2008)
5. Selected for ‘**INSPIRE FELLOWSHIP-2011-12**’ by **DST**, New Delhi.

SOFTWARE PROFICIENCY:

Languages: Verilog, VHDL

Operating Systems: Windows, XP

Simulation Tools: Xilinx, Cadence, Mentor graphics, Tanner Tools.

INDUSTRIAL TRAINING:

1. One month training from BHARAT SANCHAR NIGAM LIMITED at Durgapur.
2. Two weeks training from PHILLIPS CARBON BLACK LIMITED at Durgapur.

CONFERENCE, SEMINAR & WORKSHOP ORGANIZED

Seminar/ workshop/ Conference	Name of Seminar/workshop	Dura tion (day s)	Sponsore d by	Venue	Duration	Role
Seminar	Embedded system & technology	1	CU, EDS & IEEE Kol, Chp.	ECE, HIT, Haldia	2006 (18 March)	Organizer
Seminar	Explosive detection	1	HIT	ECE, HIT, Haldia	2007 (19 May)	Organizer & Paper

						presenter
workshop	Winter school on Embedded system	4	HIT	ECE, HIT, Haldia	2010	Organizer
National conference	NCACD 2011	2	IET, CSIR, DRDO	ECE, HIT, Haldia	5-6 Nov, 2011	Treasurer
National conference	NCACD 2012	2	CSIR, DRDO	ECE, HIT, Haldia	29-30 Sep-2012	Treasurer
Workshop	Winter school on Microcontrollers and Embedded systems	7	HIT, Haldia	ECE, HIT, Haldia	6 -12 February, 2017	Organizer
International Conference	International Conference on Communication, Devices and Computing (ICCDC 2017)	2	ISRO, CSIR, DRDO	ECE dept.	2-3 Nov. 2017	Treasurer
International Conference	2 nd Int. Conference on Information Technology and Applied Mathematics (ICITAM 2019)	2	HIT, Haldia	CSE & SAS dept.	7-9, March, 2019	Organizer
International Conference	International Conference on Communication, Devices and Computing (ICCDC 2019)	2	ISRO, DRDO	ECE dept.	14-15, March, 2019	Joint-Convenor
International Conference	3 rd International Conference on Communication, Devices and Computing (ICCDC 2021)	2		ECE Dept.	16-18, August, 2021	Publication Chair
Online FDP	Emerging Trends in IoT Enabled Wireless Communication	5		Dept. of ECE, HIT, Haldia	8-12 th August, 2022	Organizer
International Conference	4 th International Conference on Communication, Devices and Computing (ICCDC 2023)	3		ECE Dept. HIT Haldia	1-3, March, 2023	Publication Chair
National Symposium	National Symposium on IoT and Cloud Computing (NSIC2025)	2	SERB fund 1.7L SSY/2024 /001823	ECE Dept. HIT Haldia	9-10, Jan, 2025	Convenor

MOOCS CCOURSE ATTENDED

Name of MOOCs Course	Name of Course	Duration (days)	Name of Resource Person	Credit	Duration	Role
NPTEL	Hardware modeling using Verilog	8 weeks	Prof. Indranil Sengupta, IIT KGP	3	21 Aug.- 22 Oct., 2017	Mentor and Examinee (57%) certificate

NPTEL	An Introduction to Coding Theory	8 weeks	Prof. Adrish Banerjee	3	Feb-April, 2018	Mentor
NPTEL	Digital Circuits	12 weeks	Prof. Santanu Chattopadhyay	3	July-Oct 2024	Mentor

CONFERENCE, SEMINAR & WORKSHOP PARTICIPATION:

Seminar/ workshop/ Conference	Name of Seminar/workshop	Duration (days)	Sponsored by	Venue	Duration	Role
workshop	Matlab	3	TEQIP	EE, HIT, Haldia	2006 (16-18 Jun)	Participant
workshop	Microwave engineering & antennas	5		ECE, CEMK, Kolaghat	2006 (17-21 July)	Participant
National Conference	Application of operations research in management science	2	AICTE	MBA, HIT, Haldia	2007 (26-27 Dec)	Participant
workshop	PSPICE	2	TEQIP	EE, HIT, Haldia	2007 (9-10 March)	Participant
International Conference	Information Technology	3	HIT	CS & I, HIT, Haldia	2007 (19-21 March)	Participant
workshop	Technology CAD for VLSI Design	3	IIT, KGP	EC&T, IIT Kharagpur	2008	Participant
Summer school	Image and Video Processing	15	MHRD	EC&T, IIT Kharagpur	2008 (June 30- 11 July)	Participant
workshop	Introduction of VLSI design flow with SYNOPSIS tool	5	AICTE	W.B.U.T. Kolkata	2008 (21-25 July)	Participant
workshop	Trends of VLSI Design Tools	10	MHRD	BESU, Howrah.	2009 (4-10 Jan)	Participant
workshop	Cadence tools applications in VLSI	3	MSIT	MSIT, Kolkata	2010 (5-7 Sep)	Participant
workshop	High Impact Teaching Skill	5	Wipro	HIT, Haldia	2010 (26-30 July)	Participant
workshop	National Workshop on Scilab	3	MHRD	HIT, Haldia	27-29 Dec, 2010	Participant
workshop	Advanced Workshop on MISSION 10X	2	Wipro Technologies	HIT, Haldia	2010 (26-27 July)	Participant
Workshop	FPGA PROTOTYPING Using VERILOG	5	IIT, KGP	CSE, IIT Kharagpur	(25-30 Jun) 2012	Participant
Workshop	Microcontroller & Embedded System	5	IIT, KGP	CSE, IIT Kharagpur	1-7 July, 2013	Participant
Faculty Development Programme	Emerging Trends in Computing and Commun. (ETCN-15)	7	HIT, Haldia	School of ECI	5 -11 January, 2015	Participant
Faculty Development	Bridging gap between Academia and	7	HIT, Haldia	IIPC & TPO cell	5 -11 February,	Participant

Programme	Industry				2015	
Short Term Course	Advanced Communication and Signal Processing (ACSP-2015)	8	HIT, Haldia	ECE dept.	15-22 June, 2015	Participant
Webinar	VLSI devices for biomedical applications	1		Dept. of ECE, Pailan College of Management & Technology	15th June, 2020	Participant
International Webinar	Evidence-Based Lifestyle modification through Yoga in Covid-19 Pandemic (IWEVLMTYCov19)	2		Dept. of Yogic Art & Science, Vinaya Bhavana and Visva-Bharati Library Network (VBLN), Visva-Bharati,	19-20th June, 2020	Participant
Int. Virtual Conference webner	Wearable Technologies & Applications Emerging Trends and Innovations, WeTA2020	2		Vellore Institute of Technology	26-27, June, 2020	Participant
Online Faculty Development Programme	Multidisciplinary Trends in Science and Technology for Sustainable Development (A Post COVID - 19 Perspective)	6		Dept. of Basic Science and Humanities, Narula Institute of Technology	22-27 June, 2020	Participant
Online Faculty Development Programme	Signal, Image and Video Processing (SIVP 2020)	5		Dept. of ECE, Narula Institute of Technology	23-27 June, 2020	Participant
Online Faculty Development Programme	Research and Technical Challenges in Energy and Power System (RTCEPS 2020)	6		Dept. of EE, Narula Institute of Technology	29/06/20-04/07/20	Participant
National Webinar	Online Education in the Changing Times: Problems and Prospects	2		Vidyasagar University, Midnapore, West Bengal.	7- 8th July, 2020	Participant
International Webinar	Artificial Intelligence in cloud computing and IoT	1		Galgotias University	18th July, 2020	Participant
Webinar	High frequency applications of communication	1		Dept. of ECE, Pailan College of Management & Technology	21 st July, 2020	Participant
Online FDP	Wireless Communication	12	MEITY GOI	Indian Institute of Technology	27 July to 07 Aug,	Participant

	Technologies for IoT			Guwahati, and CIT Kokrajhar	2020	
Online FDP	Recent Trends in Internet of Things (IoT) and Embedded systems Based Monitoring and Control of Distributed Systems	6		Dept. ECE, Narula Institute of Technology	10.08.20-15.08.20	Participant
Online FDP	Recent Trends in Industrial and Biomedical Instrumentation	7		Dept. AEIE, Haldia Institute of Technology	02.09.20 to 08.09.20	Participant
Online FDP	Internet of Things	5	ATAL, AICTE	Dept. of CSE & IT, Anna University	21.09.20-25.09.20	Participant
Online FDP	Business Analytics	6	AICTE Sponsored	Dept. CSE, MCKV Institute of Technology	12.10.20-17.10.20	Participant
National Webinar	Recent Advancement on System Design towards 5G Communication (RASDT5C 2021)	3		Dept. of ECE, HIT, Haldia	11.01.21-13.01.21	Participant
National Webinar	Machine Learning & IOT	1		HIT, Haldia	24.06.21	Participant
Online FDP	Research Issues in VLSI Design and Testing	5	ATAL, AICTE	Govt. College of Engineering, Srirangam	02.08.21-06.08.21	Participant
Online Workshop	How to Conduct the Student Induction (SIP) Program	1		AICTE	20.09.21	Participant
Online Refresher Course	Recent Trends in VLSI Design	5	Special Manpower Development Program	Dept. of ECE, National Institute of Technology Meghalaya	27.09.21-01.10.21	Participant
Webinar	The Story of Alice and Bob	1	Dept. of Higher Edu &	JBNSTS-VP	29.09.21	Participant

			GoWB, Vigan Prasar			
Seminar (offline)	National Seminar on National Education Policy 2020	1		HIT and GIST, Haldia	22.11.21	Participant
Online FDP	Artificial Intelligence (AI) in VLSI Chip DESIGN	5	AICTE -ATAL	KONERU LAKSHMAIAH EDUCATION FOUNDATION	6.12.21- 10.12.21	Participant
Webinar	National Intellectual Property Awareness Mission (NIPAM)	1	NIPAM Team, Intellec tual Propert y India	HIT, Haldia	22.12.21	Participant
Online FDP	Recent Developments in IoT	5	AICTE -ATAL	IEM, Kolkata	17.01.22- 21.01.22	Participant
Online FDP	Innovations in IOT in emerging Applications	5		IITM Gwalior	12.02.22- 16.02.22	Participant
Online FDP	Intellectual Property Management at Early Stage of Innovation & Start- ups	6		Dept. of EE, NIT, Agartala	21.02.22- 26.02.22	Participant
FDP	Additive Manufacturing and Embedded System	6	AICTE -IDEA Lab	HIT Haldia	17-24 th May 2022	Participant
Online FDP	Scope for multidisciplinary Research and Education (SMRE 2022)	28 days	IICChE	IQAC HIT	23-07-22 to 14- 08-22	Participant
Online FDP	Universal Human Values	5	UGC	AICTE	26-09-22 to 30-09- 22	Participant
Online FDP	AIAMLCC2023	5		CSE, HIT, Haldia	10-14 th July, 2023	Participant
Online FDP	VLSI to System Design: Silicon to End Application Approach	5		AICTE, ARM	31July- 4 Aug., 23	Participant
Online FDP	Recent Advancement on Microwave and mmWave Communication	5		ECE Dept. HIT	8-12 April, 2024	Participant

Online FDP	Recent Trends in VLSI Design Using Nanotechnology	5	AICTE -ATAL	MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY	25.11.24-30.11.24	Participant
Online FDP	Emergence of Cloud Computing, Cloud Technologies and Recent Trends	6	AICTE -ATAL	Department of IT, Technology, Techno International New Town	13-01-25 to 18-01-25	Participant
Online FDP	Semiconductor	6	AICTE -ATAL	ABACUS INSTITUTE OF ENGINEERING AND MANAGEMENT	27-01-25 to 01-02-25	Participant

References:

1. Prof. (Dr.) Jaydeb Bhaumik

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2. Dr. Soma Barman

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3. Dr. Prabir Saha

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4. Prof. (Dr.) Indrajit Chakrabarti

Professor
Electronics and Electrical Communication Engineering

Indian Institute of Technology,
Kharagpur-721302
Paschim Medinipur, West Bengal, India
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PERSONAL PROFILE:

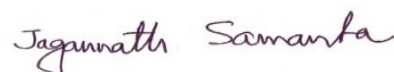
Father's Name : Late Abinash Samanta
Mother's Name : Late Radharani Samanta
Permanent Address : Vill+PO:-Sabang Shyamsundar Pur, P.S:-Sabang
Dist:- Paschim Medinipur, Pin-721155, West Bengal
Corresponding Address: D2, 4th floor, Azadhindfort, Azadhindnagar, P.O.-Township,
Haldia, PS-Haldia, Purba Medinipur, Pin-721607, West Bengal
Unique Faculty ID : WBUT-57-0010, AICTE ID:1-448638381
Date of Birth : 18-03-1983
Sex : Male
Marital Status : Married, having two daughters
Nationality : Indian
Languages Known : English, Bengali & Hindi.
Strength : a) Hard Working.
b) Disciplined.
c) Good Time Management skill.

Declaration:

I hereby declare that the above-mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

Date: 06/03/2025

Place: Haldia



(Jagannath Samanta)