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Address: Purba Medinipur ,West Bengal,India - 721657

Expertise

Telecommunications

VLSI

Work experience

1. Haldia Institute of Technology 2014 — Present

Assistant Professor
Purba Medinipur

2. Haldia Institute of Technology 2014 — 2014

Assistant Professor
Purba Medinipur

Education

1. M. Tech - 2013

Haldia Institute of Technology

Patent

1. The sentimental based disease estimation and health risk prediction system

Inventor(s): Rajrupa Metia, Santanu Maity, Razia Sultana, Amit Bhattacharya, Assignee: Haldia Institute of Technology

Published: 2022-07-08

2. LOW-POWER VLSI ARCHITECTURE FOR EDGE COMPUTING IN IOT ENVIRONMENTS

Inventor(s): Mr. Eswararao Boddepalli 2 . Ms. Rajrupa Metia 3 . Mr. Biswajit Das 4 . Mr. Santanu Maity 5 . Mrs. Razia Sultana, Assignee:

Published: 2024-02-02

3. Edge AI-Enabled IOT system for real time anomaly Detection and predictive maintenance in industrial environments

Inventor(s): Dr, Ritwik Halder, Dr Arpita Mazumder, Dr, Santanu Maity, Dr. Amit Bhattacharyya, Dr. Pinaki Satpathy, Razia Sultana, Kosalaya Chakrabarti , Mr. Devadatta Das, Assignee:

Published: 2025-04-04

Publication

1. Innovative Technique For Generation Of X-Ray Based On Molecular Quantum Harmonic Oscillator And Subsequent Application In Determination Of Carcinoma Of Lungs And Breast Cells Using Gold Nanowire Network

Sachindeb Jana , Razia Sultana , Rajrupa Metia , Kosalaya Chakrabarti , Angsuman Sarkar
African Journal of Biomedical Research , Volume Vol. 27(3s), Year 2025, Pages 7062- 7076

2. Performance Analysis of Modified Karatsuba Multiplier and Application

R. Sultana

Performance Analysis of Modified Karatsuba Multiplier and Application, Volume , Year 2023, Pages

3. An Improved generalized Karatsuba Multiplier in GF(2M) field and it's convolution Application

R. Sultana

Journal of Emerging technologies and innovative Research, Volume 9, Year 2022, Pages

4. Determination of Linear Far field Pattern in Triangular Index Optical fiber for the Fundamental Transmission Mode

R. Sultana, Jayanta Kumar Bag, Sayani Ghosh, Tilak Mukherjee, Kushal Roy

The Journal of Critical Reviews, Volume 7, Year 2020, Pages 2847-2852

5. Simulative Investigation on Wavelength Division Demultiplexer with Single mode Directional Couplers

Moumita jana, Razia Sultana, Akinchan Das, Banibrata Bag
Turkish Journal of computer and Mathematics Education, Volume 11, Year 2020, Pages 1904-1912

6. Design and Implementation of 4 bit Vedic Multiplier

A. Maity, K. Chakraborty, R. Sultana
International Journal of Emerging in Science and Technology, Volume 03, Year 2016, Pages 3865-3868

7. Design and Implementation of High speed low power Multiplier using Reversible logic

K. Chakraborty, A. Maity, S. Maity, R. Sultana
International Journal of Emerging in Science and Technology, Volume 3, Year 2016, Pages 3859-3864

8. Comparative analysis and study on 4 bit RCA and CSA using CMOS logic

S. R. Mondal, M. Bhowmik, S. Maity, R. Sultana
International journal for soft computing and Engineering, Volume 4, Year 2015, Pages

9. Design an 8 bit Microprocessor using VHDL

S. Metia, A. K. Pramanik, R. Sultana
American journal of Electronics and Communication, Volume 2, Year 2015, Pages 122-126

10. High Performance Carry Skip Adder using Reversible Logic

Monalisha Bhowmik, Razia Sultana
International Journal of VLSI and Embedded Systems-IJVES , Volume , Year 2015, Pages

11. FPGA based Modified Karatsuba Multiplier

Jagannath Samanta, Razia Sultana, Jaydeb Bhaumik
International Conference on VLSI and signal Processing, Volume , Year 2014, Pages 1-6

12. Comparison of different design techniques of XOR &AND; gate using EDA simulation tool

R. Sultana, J. Samanta
International Journal of VLSI and Embedded System, Volume 4, Year 2013, Pages